Amendments to the Claims

This listing of claims will replace all prior version, and listings, of claims in the application.

Listing of Claims:

1. (Currently amended) A single I/O interface comprising:

a host port coupled to a first chipset; and

a peripheral port coupled to a second chipset, wherein the host port and the peripheral port are defined using predetermined signals.

2. (original) The interface of claim 1 wherein the host and peripheral ports are USB ports.

3. (Currently amended) The interface of claim 1 wherein two connected devices utilizing the single I/O interface can have a peer-to-peer connection via the host port and peripheral port.

4. (Currently amended) The interface of claim 1 wherein two connected devices utilizing the single I/O interface can have a one-to-many relationship via either the host port and/or the peripheral port.

5. (Original) The interface of claim 1 wherein a device only needs one physical I/O port via the connector.

6. (Original) The interface of claim 1 wherein the predetermined signals comprise host differential data lines and peripheral differential data lines.

7. (Currently amended) A USB network comprising:

a first device; the first device including a single I/O interface, the interface including a host port coupled to a first chipset; and a peripheral port coupled to a second chipset, wherein the host port and the peripheral port are defined using predetermined signals; and

a second device for communicating with the first device, the second device using the predetermined signals.

8. (Original) The USB network of claim 7 wherein the predetermined signals are within a standard.

9. (Original) The USB network of claim 8 wherein the standard comprises the universal serial bus (USB) standard.

10. (Original) The USB network of claim 9 wherein the first and second devices can be any of a camera, computer, personal digital assistant, laptop device, handheld device, printer, and cellular telephone.

11. (Original) The USB network of claim 7 wherein the predetermined signals comprise host differential data lines and peripheral differential data lines.

12. (Currently amended) A device comprising:

a processor; and

a single I/O interface coupled to the processor, the ~~connector~~ single I/O interface comprising a host port coupled to a first chipset; and a peripheral port coupled to a second chipset, wherein the host port and the peripheral port are defined using predetermined signals.

13. (Original) The device of claim 12 wherein the single I/O interface requires a connection to only one physical I/O port if the device is coupled to a device with a connector that includes a host port and a peripheral port which are defined using the predetermined signals.

14. (Original) The device of claim 12 wherein the predetermined signals comprise host differential data lines and peripheral differential data lines.